[0074] What is claimed is:

1. A method comprising:

selecting values for a field of a micro-operation based at least upon bits of a field of a micro-operation template, wherein the number of said bits is fewer than the number of bits in said field of said micro-operation.

2. The method of claim 1, wherein selecting said values includes selecting said values if said micro-operation is a fused micro-operation.

3. The method of claim 2, wherein selecting said values includes selecting said values for an op-code of said micro-operation.

4. A method comprising:

generating micro-operation templates for micro-operations, said templates including bits to be used to select values for a particular field of said micro-operations, wherein the number of said bits in said templates is smaller than the maximal number of bits of said particular field.

5. The method of claim 4, wherein said particular field is an op-code.

6. The method of claim 4, wherein said micro-operations are fused micro-operations.

7. A method comprising:

decoding an instruction into a fused micro-operation, including selecting values of a field of said fused micro-operation based solely upon an indication that said instruction is not being decoded into a simple micro-operation.

8. The method of claim 7, further comprising:

generating said indication for said instruction from one or more fields of a micro-operation template.

9. The method of claim 7, wherein selecting values of said field includes selecting values of an operand of said fused micro-operation.

10. A method comprising:

decoding an instruction into a fused micro-operation, including selecting values of a first field of said fused micro-operation based solely upon an indication that said instruction is not being decoded into a simple micro-operation

and a value decoded from a field of a micro-operation template that is used to select values of a second field of said fused micro-operation.

11. The method of claim 10, wherein said first field is an operand of said fused micro-operation.

12. The method of claim 10, wherein said second field is an op-code of said fused micro-operation.

13. A method comprising:

decoding a field of a micro-operation template that is used to select values of a field of a fused micro-operation in order to distinguish between different micro-operation templates that are addressed by instructions during decoding of said instructions into fused micro-operations.

14. The method of claim 13, wherein said field of said fused micro-operation is an op-code of said fused micro-operation.

15. The method of claim 13, wherein said field of said fused micro-operation is an operand of said fused micro-operation.

16. A method comprising:

addressing a micro-operation template by one or more instructions to be decoded into one or more fused micro-operations and by one or more instructions to be decoded into one or more simple micro-operations.

17. The method of claim 16, further comprising:

generating for a particular instruction that addresses said micro-operation template an indication whether said particular instruction is to be decoded into a fused micro-operation or into a simple micro-operation.

18. The method of claim 17, wherein generating said indication comprises generating said indication from one or more fields of said micro-operation template and from bits extracted directly from said particular instruction.

19. A method comprising:

selecting values of a field of a micro-operation from a first set of physical traces if said micro-operation is simple and from a second set of physical traces if said micro-operation is fused, where said micro-operation is generated from a

micro-operation template that is addressed by one or more instructions to be decoded into one or more fused micro-operations and by one or more instructions to be decoded into one or more simple micro-operations.

20. The method of claim 19, wherein selecting said values comprises selecting said values based at least upon an indication whether an instruction from which said micro-operation is being decoded is being decoded into a fused micro-operation or into a simple micro-operation.

21. The method of claim 19, wherein said field is an operand of said micro-operation.

22. A processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field; and

a multiplexer to select values for said particular field based at least upon bits of a field of said micro-operation template, wherein the number of said bits is fewer than the number of bits in said particular field.

23. The processor of claim 22, wherein said particular field is an op-code of said fused micro-operation.

24. The processor of claim 22, wherein said multiplexer is to select values for said particular field also based upon an indication that said instruction is not being decoded into a simple micro-operation.

25. A processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field; and

a multiplexer to select values for said particular field based solely upon an indication that said instruction is not being decoded into a simple micro-operation.

26. The processor of claim 25, wherein said particular field is an operand of said fused micro-operation.

27. The processor of claim 25, wherein said indication comprises bits of a field of said micro-operation template.

28. The processor of claim 25, wherein said instruction decoder further comprises:

a decoder to generate said indication from two or more fields of said micro-operation template and from bits extracted directly from said instruction.

29. A processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field;

a decoder to decode a value from a field of said micro-operation template; and

a multiplexer to select values for said particular field based solely upon said value and an indication that said instruction is not being decoded into a simple micro-operation.

30. The processor of claim 29, wherein said field of said micro-operation template is used to select values of an op-code of said fused micro-operation.

31. The processor of claim 29, wherein said particular field is an operand of said fused micro-operation.

32. The processor of claim 29, wherein said indication comprises bits of another field of said micro-operation template.

33. The processor of claim 29, wherein said instruction decoder further comprises:

a decoder to generate said indication from two or more additional fields of said micro-operation template and from bits extracted directly from said instruction.

34. A processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations.

35. The processor of claim 34, wherein said micro-operation template includes a field having a value that identifies that both a fused micro-operation and a simple micro-operation can be generated from said micro-operation template.

36. The processor of claim 34, wherein said instruction decoder further comprises:

a decoder to generate an indication for a particular instruction from two or more fields of said micro-operation template and from bits extracted directly from said particular instruction, wherein said indication is an indication whether said particular instruction is to be decoded into a fused micro-operation or into a simple micro-operation.

37. An apparatus comprising:

a voltage monitor; and

a processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field; and

a multiplexer to select values for said particular field based at least upon bits of a field of said micro-operation template, wherein the number of said bits is fewer than the number of bits in said particular field.

38. The apparatus of claim 37, wherein said particular field is an op-code of said fused micro-operation.

39. The apparatus of claim 37, wherein said multiplexer is to select values for said particular field also based upon an indication that said instruction is not being decoded into a simple micro-operation.

40. An apparatus comprising:

a voltage monitor; and

a processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field; and

a multiplexer to select values for said particular field based solely upon an indication that said instruction is not being decoded into a simple micro-operation.

41. The apparatus of claim 40, wherein said particular field is an operand of said fused micro-operation.

42. The apparatus of claim 40, wherein said indication comprises bits of a field of said micro-operation template.

43. The apparatus of claim 40, wherein said instruction decoder further comprises:

a decoder to generate said indication from two or more fields of said micro-operation template and from bits extracted directly from said instruction.

44. An apparatus comprising:

a voltage monitor; and

a processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by an instruction during decoding of said instruction into a fused micro-operation having a particular field;

a decoder to decode a value from a field of said micro-operation template; and

a multiplexer to select values for said particular field based solely upon said value and an indication that said instruction is not being decoded into a simple micro-operation.

45. The apparatus of claim 44, wherein said field of said micro-operation template is used to select values of an op-code of said fused micro-operation.

46. The apparatus of claim 44, wherein said particular field is an operand of said fused micro-operation.

47. The apparatus of claim 44, wherein said indication comprises bits of another field of said micro-operation template.

48. The apparatus of claim 44, wherein said instruction decoder further comprises:

a decoder to generate said indication from two or more additional fields of said micro-operation template and from bits extracted directly from said instruction.

49. An apparatus comprising:

a voltage monitor; and

a processor to execute instructions, the processor comprising:

an instruction decoder including at least:

a programmable logic array to store a micro-operation template to be addressed by one or more instructions that are to be decoded into one or more fused micro-operations and by one or more instructions that are to be decoded into one or more simple micro-operations.

50. The apparatus of claim 49, wherein said micro-operation template includes a field having a value that identifies that both a fused micro-operation and a simple micro-operation can be generated from said micro-operation template.

51. The apparatus of claim 49, wherein said instruction decoder further comprises:

a decoder to generate an indication for a particular instruction from two or more fields of said micro-operation template and from bits extracted directly from said particular instruction, wherein said indication is an indication whether said particular instruction is to be decoded into a fused micro-operation or into a simple micro-operation.